

CLAIMS

What is claimed is:

- 1 1. A method comprising:
 - 2 receiving circuit analysis results;
 - 3 identifying a duplicate circuit analysis result among the received circuit analysis
 - 4 results; and
 - 5 outputting a list of circuit analysis results that excludes the duplicate circuit
 - 6 analysis result.
- 1 2. The method of claim 1, further comprising:
 - 2 sorting the circuit analysis results.
- 1 3. The method of claim 2, wherein the circuit analysis results are sorted alphabetically.
- 1 4. The method of claim 2, further comprising:
 - 2 comparing each of the circuit analysis results with an adjacent circuit analysis
 - 3 result.
- 1 5. The method of claim 2, wherein the circuit analysis results are sorted based on types of
2 circuit analysis results.
- 1 6. The method of claim 5, wherein the types of circuit analysis results comprise a type of
2 result configured to enable detection of latch design defects.
- 1 7. The method of claim 5, wherein the types of circuit analysis results comprise a type of
2 result configured to enable detection of dynamic gate design defects.
- 1 8. The method of claim 5, wherein the types of circuit analysis results comprise a type of
2 result configured to enable detection of clock design defects.
- 1 9. The method of claim 5, wherein the types of circuit analysis results comprise a type of
2 result configured to enable detection of pseudo-NMOS gate design defects.

- 1 10. The method of claim 5, wherein the types of circuit analysis results comprise a type of
2 result configured to enable detection of pass-FET design defects.
- 1 11. A system comprising:
2 memory configured to store program code; and
3 at least one processor that is programmed by the program code to:
4 identify a duplicate circuit analysis result; and
5 output a list of circuit analysis results that excludes the duplicate circuit
6 analysis result.
- 1 12. The system of claim 11, wherein the at least one processor is further programmed to
2 sort the circuit analysis results.
- 1 13. The system of claim 12, wherein the circuit analysis results are sorted alphabetically.
- 1 14. The system of claim 12, wherein the at least one processor is further programmed to
2 compare each of the circuit analysis results with an adjacent circuit analysis result.
- 1 15. The system of claim 12, wherein the circuit analysis results are sorted based on types
2 of circuit analysis results.
- 1 16. The system of claim 15, wherein the types of circuit analysis results comprise a type
2 of result configured to enable detection of latch design defects.
- 1 17. The system of claim 15, wherein the types of circuit analysis results comprise a type
2 of result configured to enable detection of dynamic gate design defects.
- 1 18. The system of claim 15, wherein the types of circuit analysis results comprise a type
2 of result configured to enable detection of clock design defects.
- 1 19. The system of claim 15, wherein the types of circuit analysis results comprise a type
2 of result configured to enable detection of pseudo-NMOS gate design defects.

1 20. The system of claim 15, wherein the types of circuit analysis results comprise a type
2 of result configured to enable detection of pass-FET design defects.

1 21. A computer readable medium having computer-readable instructions configured to:
2 receive circuit analysis results;
3 identify a duplicate circuit analysis result among the received circuit analysis
4 results; and
5 output a list of circuit analysis results that excludes the duplicate circuit analysis
6 result.

1 22. The computer readable medium of claim 1, wherein the computer-readable
2 instructions are further configured to:
3 sort the circuit analysis results; and
4 compare each of the circuit analysis results with an adjacent circuit analysis result.

1 23. A system comprising:
2 means for receiving circuit analysis results;
3 means for identifying a duplicate circuit analysis result among the received circuit
4 analysis results; and
5 means for outputting a list of circuit analysis results that excludes the duplicate
6 circuit analysis result.

1 24. The system of claim 23, further comprising:
2 means for sorting the circuit analysis results; and
3 means for comparing each of the circuit analysis results with an adjacent circuit
4 analysis result.